Evolutionary Synthesis of Quantum-dot Cellular Automata Circuits

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Until recently micrometer was the basic scale for the integration of the CMOS technology. In the past few years this scale has moved to the next level – nanometer scale, but there are fundamental limits like electron thermal energy or tunneling leakage through gate oxide. It is possible that the limits of the CMOS technology are almost reached. To solve this problem, a lot of studies on the nanometer scale have been done. One of them was demonstrated in the early 1990s by C. S. Lent, et al.. They introduced the representation of binary logic values as configurations of a pair of electrons contained in a quantum-dot cell. Later studies of the interactions between such cells arranged in Quantum-dot Cellular Automata (QCA) resulted in the implementation of simple logic devices. There have even been attempts at the implementation of Quantum-dot Field Programmable Gate Arrays. All in all, QCA have a large potential in the development of circuits with high space density and low heat dissipation and promise the development of faster computers with lower power consumption. As a contrast to conventional technologies, QCA do not codify information by means of electric current flow, but rather by the configuration of electrical charges in the interior of the cells. The Coulomb interaction between cells is responsible for the flow of information. Standard design approaches, typically used in CMOS design, therefore need to be revised.

In this article we propose the use of Genetic Algorithms (GA) for automatic synthesis of QCA circuits. Inputs to our GA were the positions of inputs and outputs of the logic device, its maximal size, as well as the logic function we wanted the logic circuit to perform. For reasons of stability and energy flow we typically employed three inputs and also three outputs. By means of GA we managed to design logic devices for all two input binary logic functions. It has to be stressed out that all are based around a single control signal (i.e. the inter-dot barriers are raised and lowered in all cells concurrently) and that the GA obtained logic devices are optimal in view of the number of employed QCA cells. The device behavior analysis was performed in the QCADesigner tool. An example of a GA synthesized logic device performing the NOR logic function is presented in Fig. 1. Present results confirm that GA techniques may prove helpful in the research of QCA logic device design as they are capable of synthesizing optimized circuits with a reduced number of cells.

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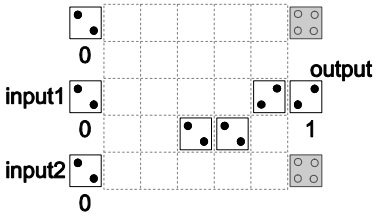

input1	input2	output
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 1. A GA synthesized logic device performing the NOR logic function. The GA parameters were the locations of possible inputs and outputs, the maximal internal size (a 5x5 grid) and the desired output logic values. The unused output locations are marked in gray.