Introduction to Reversible Logic Gates & its Application

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ABSTRACT
In current scenario, the reversible logic design attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate, New Gate sayem gate and peres gate etc. This paper present a basic reversible gate to build more complicated circuits which can be implemented in ALU, some sequential circuits as well as in some combinational circuits. It also gives brief idea to build adder circuits using the basic reversible gate like peres gate and TSG gate.

Keywords
Low-power VLSI, Low-power CMOS design, reversible logic, quantum cost, reversible counters

1. INTRODUCTION
Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where $K=1.3806505*10^{-23}m^2kg^{-2}K^{-1}$ (joule/Kelvin^{-1}) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless

2. THE CONCEPT
Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency.

3. MOTIVATION BEHIND REVERSIBLE LOGIC
High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored

4. REVERSIBLE LOGIC GATES
A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic

circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

4.1. BASIC REVERSIBLE LOGIC GATES

4.1.1 Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A ⊕ B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

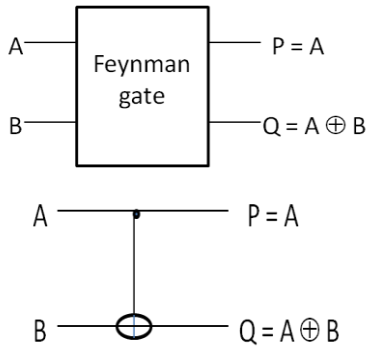

Figure 1: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1: Truth table of Feynman gates

4.1.2 Double Feynman Gate (F2G)

Fig.2 shows a 3*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A ⊕ B, R=A ⊕ C. Quantum cost of double Feynman gate is 2.

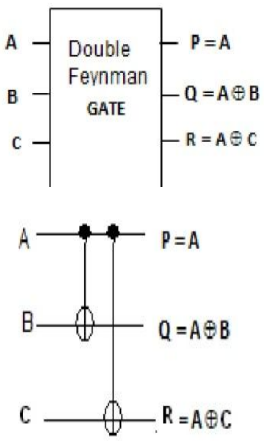

Fig 2: Double Feynman gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 2: Truth table of double Feynman gates

4.1.3 Toffoli Gate:

Fig 3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB ⊕ C. Quantum cost of a Toffoli gate is 5.

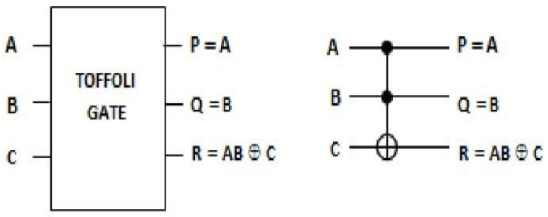

Fig 3: Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 3: Truth table of Toffoli gate

4.1.4 Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B ⊕ AC and R=A′C ⊕ AB. Quantum cost of a Fredkin gate is 5.

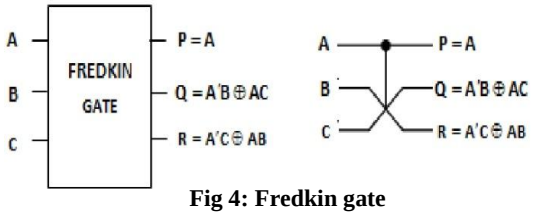

Fig 4: Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 4: Truth table of fredkin gate

4.1.5 Peres Gate

Fig 5 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A ⊕ B and R=AB ⊕ C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

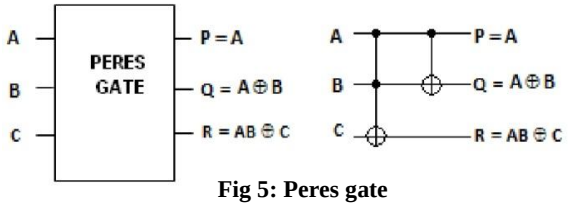

Fig 5: Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 5: Truth table of peres gate

A full- adder using two Peres gates is as shown in fig 6. The quantum realization of this shows that its quantum cost is 8 two Peres gates are used

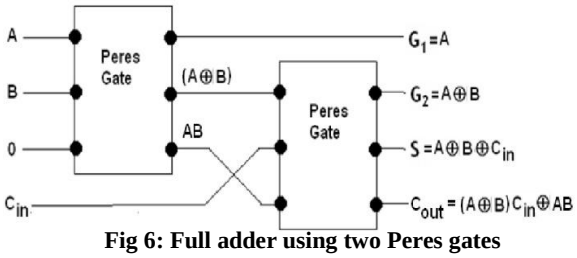

Fig 6: Full adder using two Peres gates

A single 4*4 reversible gate called PFAG gate with quantum cost of 8 is used to realize the multiplier

4.1.6 TSG gate

Fig 7 shows a 4*4 TSG gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). The output is defined by P = A, Q = A'C'⊕B', R = (A'C'⊕B')⊕ D and S = (A'C'⊕B').D⊕ (AB⊕C) Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost. It can be verified that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed TSG gate is capable of implementing all Boolean functions and can also work singly as a reversible Full adder

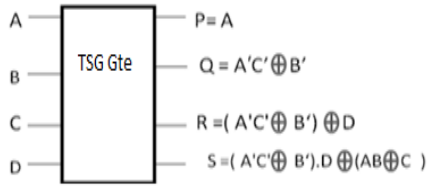

Fig 7: TSG gate

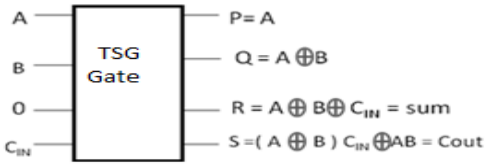

Fig 8: TSG Gate Working As Reversible Full Adder

4.1.7 Sayem gate

SG is a 1 trough 4x4 reversible gate. The input and output vector of this gate are, Iv = (A, B, C, D) and Ov = (A, A'B ⊕ AC, A'B ⊕ AC⊕ D, AB ⊕ A'C ⊕ D). The block diagram of this gate is shown in Fig 9

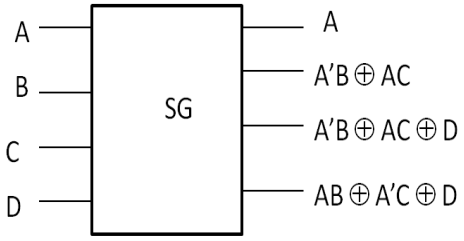

Fig 9: Sayem gate

4.1.8 D-latch

The characteristic equation of D-Latch is *Q+ =DE+E'Q*. It can be realized with one SG. It can be mapped with SG by giving E, Q, D and 0 respectively in 1st, 2nd, 3rd and 4th input of SG. Fig 10(a) shows the design of D-Latch with only Q output and Fig 10(b) shows the design of reversible D-Latch with both the output Q and Q+ .One FG is needed to copy and produce the complement of Q from SG for the design of Fig 10(b)

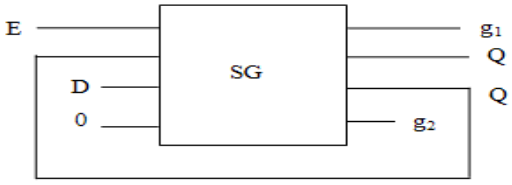

Fig 10(a): Proposed design of D-Latch with only output Q

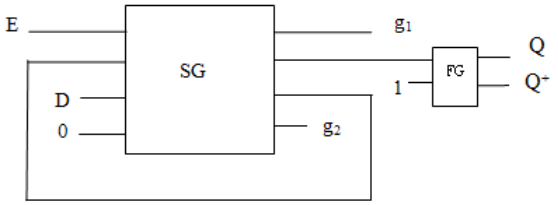

Fig 10(b): Proposed design of D-Latch with output Q and Q+

4.1.9 Reversible Positive Edge Triggered T-Flip Flop

This section includes the construction of Master-Slave T Flip-Flop using reversible gates. The truth table is shown in the Table 6. The design is shown in the Figure 11 [8]. The added Feynman gate as shown in figure to get the desired functionality of Q-1.

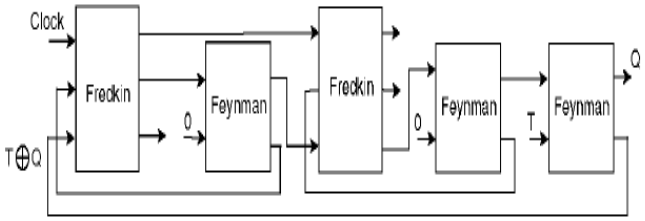

Figure 11: Reversible positive edge triggered T flip-flop

CLK	T	Q_{t-1}	Q
0	O	0	0
1	O	0	0
0	O	1	1
1	O	1	1
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	0

Table 6: positive edge triggered T flip-flop

This construction is done can be done by replacing fredkin and Feynman gate by single sayem gate The reversible realization of T Flip-flop has two SG gates and one Feynman Gate is shown in fig 12[5].

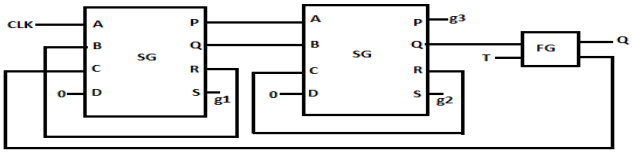

Fig 12: Reversible Positive Edge Triggered T Flip-flop

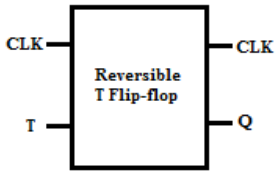

Figure 13: reversible T flip flop

5. PROPOSED 4-BIT ASYNCHRONOUS UP/DOWN COUNTER:

The reversible design of the asynchronous Up/Down Counter is shown in Fig. 14. The Up/Down operation of this reversible design is controlled by the control input UP/DOWN. When this control input is 1 the reversible design operates as an Up counter. When this control input is 0 the reversible design operates as a Down Counter

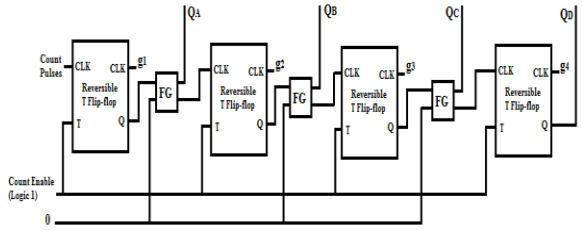

Fig 14: Proposed 4-bit Reversible Asynchronous down Counter

6. APPLICATIONS

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

1. Low power CMOS.
2. Quantum computer.
3. Nanotechnology
4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair

7. CONCLUSION

We have presented an approach to the realize the multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. The proposed asynchronous designs have the applications in digital circuits like a Timer/Counter, building reversible ALU, reversible processor etc. This work forms an important move in building large and complex reversible sequential circuits.

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