Univerza v Ljubljani

Računalniški sistemi

Seminarska naloga

Delilnik dveh dvo-bitnih števil

Ercan Canhasi, 63090404

Ljubljana, 25.11.2008

Contents

1. Introduction

1.1 Motivation

As a part of individual work assignment of a course “Računalniški Sistemi”, the seminar on quantum dot cellular automata has been prepared. Task was to design a 2 bit binary QDCA divider.
Practical work and results are presented in this report where first a short introduction on quantum dot cellular automata is given. Report then continues with analyze of problem and design of circuit with conventional binary logic gates and then with QCDA. At the end of the report personal opinions and conclusions are given.

1.2 QCA

A cellular automaton (CA) is an abstract system consisting of a uniform (finite or infinite) grid of cells. Each one of these cells can only be in one of a finite number of states at a discrete time.
in 1993, Lent et al. proposed a physical implementation of an automaton using quantum-dot cells. The automaton quickly gained popularity and it was first fabricated in 1997. Lent combined the discrete nature of both, cellular automata and quantum mechanics, to create nano-scale devices capable of performing computation at very high switching speeds and consuming extremely small amounts of power.

2. Problem definition

Since task is to divide two numbers represented in binary form, it seems reasonable to first analyze a problem from a conventional binary logic perspective and it counterpart in real design, logic gates.
In common notation division is presented as A/B = C where A and B, dividend and divisor, are inputs and C, a quotient, is the output of division. A quotient can also mean just the integer part of the result of dividing two integers. There can be a reminder also, which represents a remaining of a division, in this particular task we are omitting it, since we are just interested in binary division of two two-bite long binary numbers without remaining.

3. Realization

Binary division is similar to its decimal counterpart. In order to see whole picture of possible results of binary division on two two-bite long binary numbers let show the truth table:

Dividend		**Divisor**		**Quotient**		
a	**b**	**C**	**d**	**R1**	**R0**	**R1R0 decimal**
0	0	0	0	N	N	div by zero
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	N	N	div by zero
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	N	N	div by zero
1	0	0	1	1	0	2
1	0	1	0	0	1	1
1	0	1	1	0	0	0
1	1	0	0	N	N	div by zero
1	1	0	1	1	1	3
1	1	1	0	0	1	1
1	1	1	1	0	1	1

Division by zero:

In ordinary (real number) arithmetic, this expression has no meaning.
So it's decided to apply same reasoning here. It can be seen from truth table that division by zero is defined as NN (not number).

In actual binary gate design circuit divByZero is commonly presented by divByZero flag (bit).

R0 = abcd + abcd'+ abc'd + ab'cd' + a'bc'd
R1= ab'c'd + abc'd

As the resulting Boolean functions seem suitable for simplification by using karnaugh maps previous functions are simplified to fallowing ones:

R0 = abc + bc'd + acd'
R1 = ac'd

Now we can show to logic gate design of given functions:

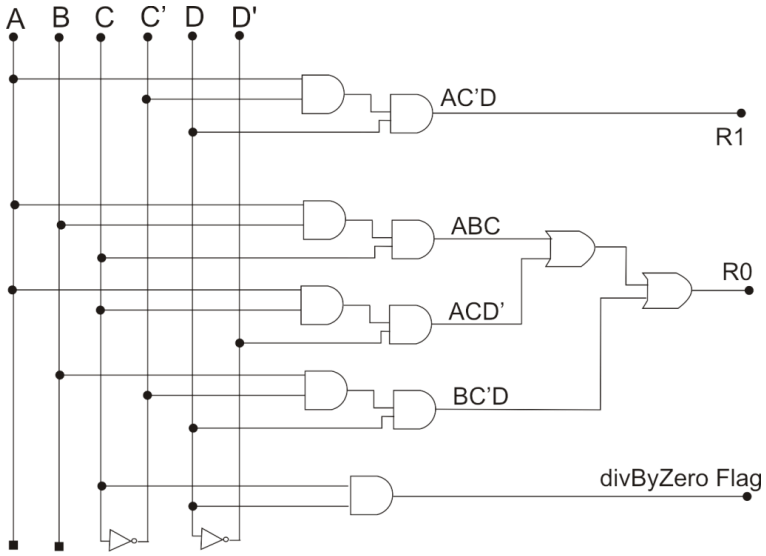

Figure 1.1 Binary logic circuit for 2 bit binary divider.

Binary logic circuit for 2 bit binary divider with divByZero flag for division by zero error is shown on Fig. 1.1. It has been tested in logic gates simulator and since it worked correctly according to truth table, the next step was to design identical circuit in QCADesigner.

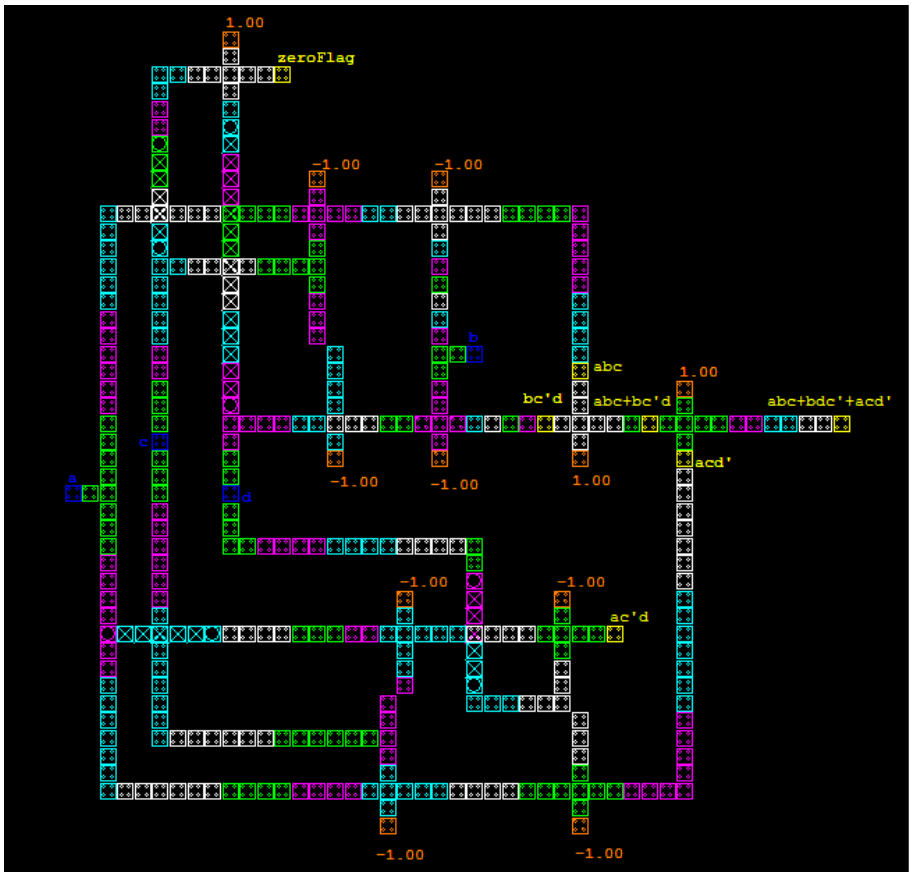

Figure 1.2 Binary logic circuit for 2 bit binary divider.

As it can be seen on Fig. 1.2 above given combinatorial logic circuit is just redesigned in QCADesigner by replacing logic gates with their counterparts in QCA. Some addition and specific problems usual for QCA are fixed, but all about this will be given in conclusion.
Some properties of realized QCD divider are:

- 4 inputs ABCD,
  - where AB are first number organized in bus named “divident”
  - and CD are bits of second number combined in bus “divisor”
- 3 main outputs
  - R0R1 are bits of output number or Quotient.
  - divByZero bit
- in design are used 397 qcda cells
- total time delay of a circuit is 4 clocks

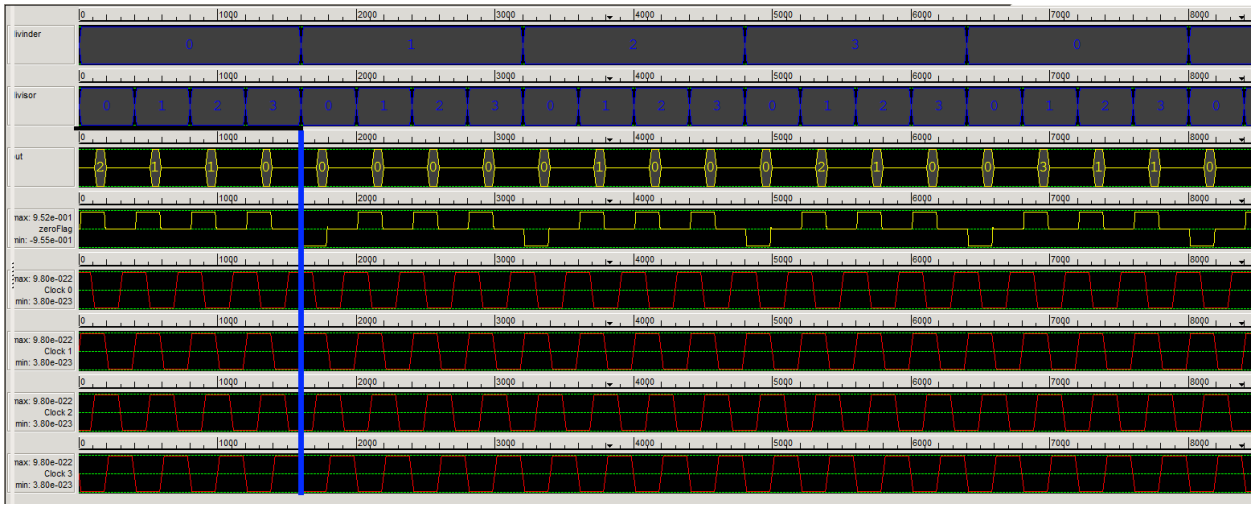

Figure 1.2 Simulation results of QCDA divider.

As it can be seen from simulation results (fig 1.2) QCDA circuit works properly. One should read simulation results from blue line forward, which means with 4 clock delay.

Simulation results can be read like on fallowing table.

Dividend	**Divisor**	**Quotient**	**divByZero**
0	0	0	0
0	1	0	1
0	2	0	1
0	3	0	1
1	0	0	0
1	1	1	1
1	2	0	1
1	3	0	1
2	0	0	0

2	1	2	1
2	2	1	1
2	3	0	1
3	0	0	0
3	1	3	1
3	2	1	1
3	3	1	1

4. Conclusion

This seminar work shows that it is possible to realize binary division in QCDA. Design of a QCDA circuit has been done in combinatorial logic way. Main difficulties faced in design process were in maintaining the optimum number of cells in separated clocks in order to have the outputs on same clock.

One should take in consideration fallowing good practices in QCADesigner:

- When cells with static polarization are used in design there should be used extra cell between fixed cells and logical gates.
- Inputs to same logic gates should be on same clock.
- Balance in numbers of cells on different clocks in a line of qca cells should be maintained.
- As an easier solution to wire crossing multi-layered design should be used.
- In multi-layered design preventing inter cellular influence can be gained by using 3 or more layers.
- Simulation results have to been read carefully, bearing in mind clock delays.

5. References

1. http://lrss.fri.uni-lj.si/sl/teaching/ont/default.asp?lc=sl
2. http://en.wikipedia.org/wiki/Quantum_dot_cellular_automaton
3. AdderDesignsandAnalysesforQuantum-Dot CellularAutomata, HeumpilCho,StudentMember,IEEE,andEarlE.Swartzlander,Jr.,Fellow,IEEE